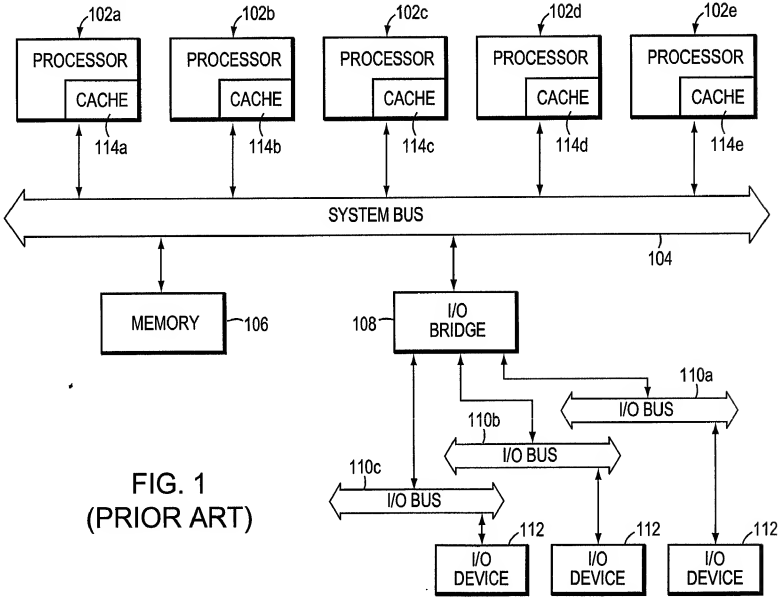

FIG. 1
(PRIOR ART)

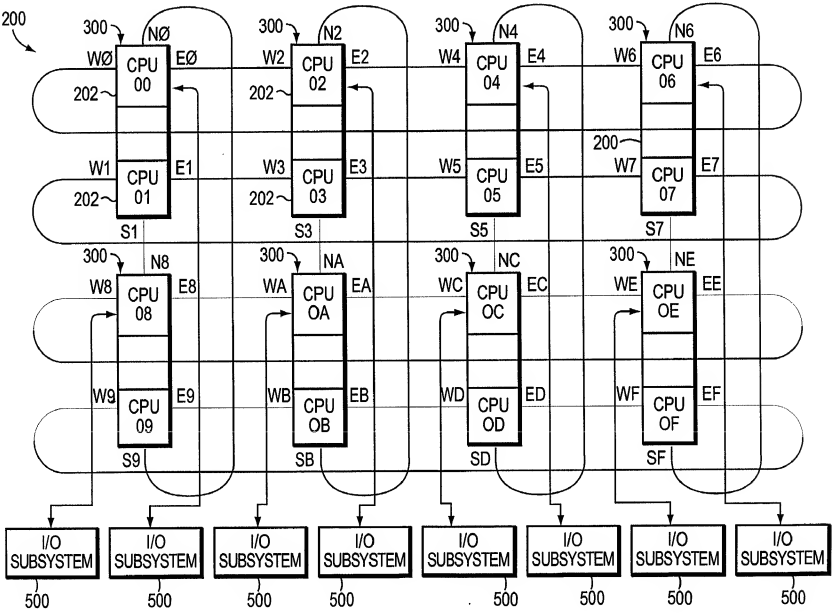
200
300
NØ
WØ
CPU 00
EØ
202
W1
CPU 01
E1
S1
N2
W2
CPU 02
E2
W3
CPU 03
E3
S3
N4
W4
CPU 04
E4
W5
CPU 05
E5
S5
N6
W6
CPU 06
E6
W7
CPU 07
E7
S7
N8
W8
CPU 08
E8
W9
CPU 09
E9
S9
NA
WA
CPU OA
EA
WB
CPU OB
EB
SB
NC
WC
CPU OC
EC
WD
CPU OD
ED
SD
NE
WE
CPU OE
EE
WF
CPU OF
EF
SF
I/O SUBSYSTEM
500

FIG. 2

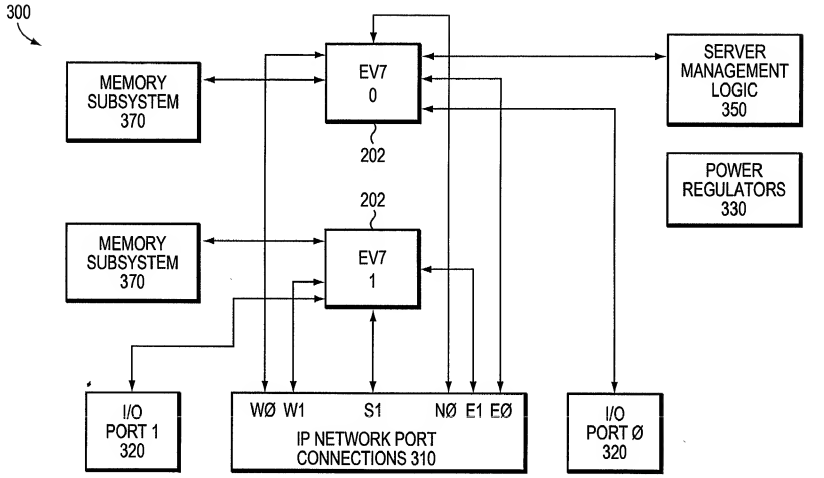

FIG. 3

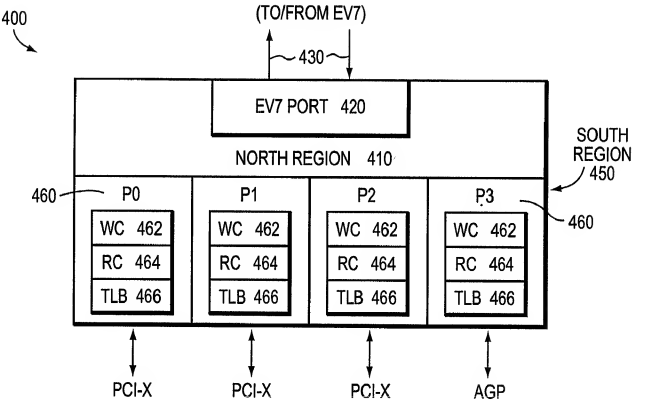

FIG. 4

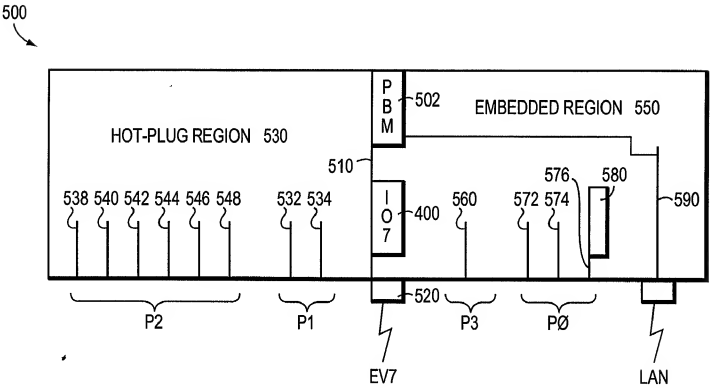

FIG. 5

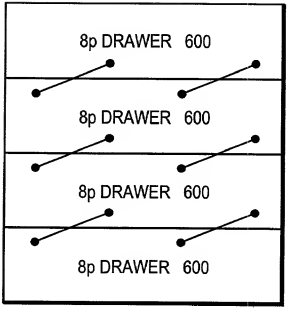

FIG. 6

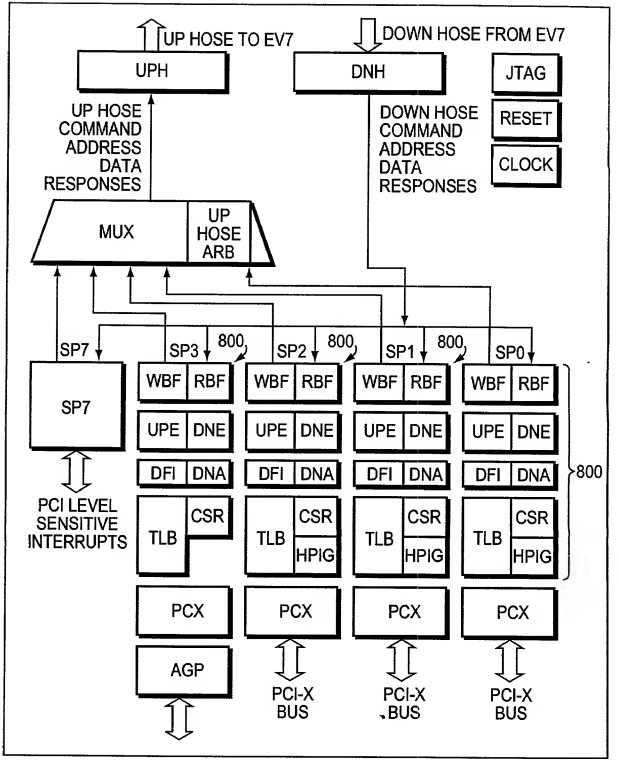
UP HOSE TO EV7
DOWN HOSE FROM EV7
UPH
DNH
JTAG
RESET
CLOCK
UP HOSE COMMAND ADDRESS DATA RESPONSES
DOWN HOSE COMMAND ADDRESS DATA RESPONSES
MUX
UP HOSE ARB
SP7
SP3
SP2
SP1
SP0
800
WBF
RBF
UPE
DNE
DFI
DNA
CSR
TLB
HPIG
PCX
AGP
PCI LEVEL SENSITIVE INTERRUPTS
PCI-X BUS

FIG. 7

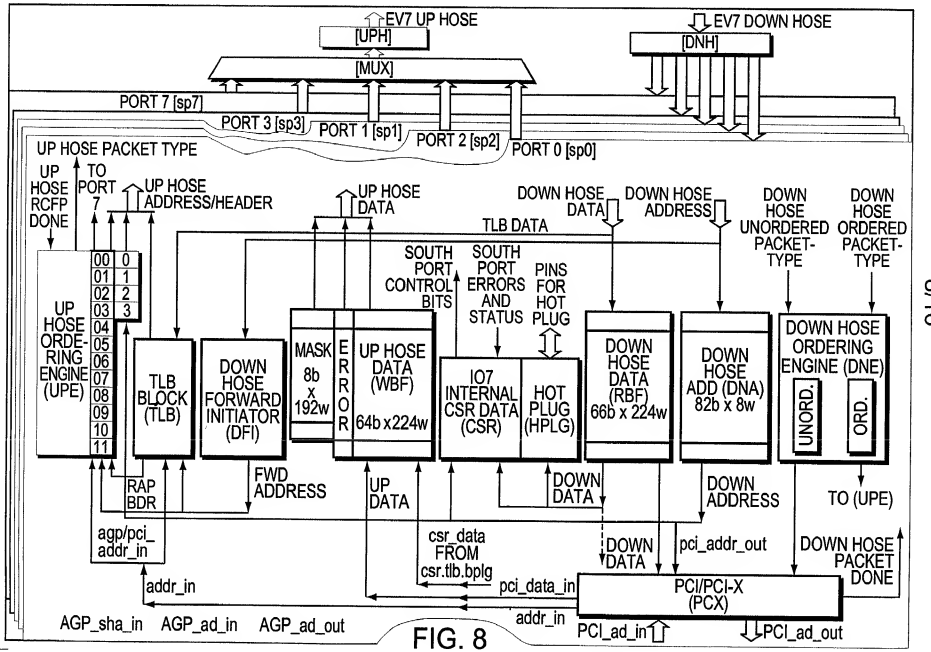
EV7 UP HOSE
[UPH]
EV7 DOWN HOSE
[DNH]
[MUX]
PORT 7 [sp7]
PORT 3 [sp3]
PORT 1 [sp1]
PORT 2 [sp2]
PORT 0 [sp0]
UP HOSE PACKET TYPE
UP HOSE RCFP DONE
TO PORT 7
UP HOSE ADDRESS/HEADER
UP HOSE DATA
DOWN HOSE DATA
DOWN HOSE ADDRESS
DOWN HOSE UNORDERED PACKET-TYPE
DOWN HOSE ORDERED PACKET-TYPE
TLB DATA
SOUTH PORT CONTROL BITS
SOUTH PORT ERRORS AND STATUS
PINS FOR HOT PLUG
00 0
01 1
02 2
03 3
04
05
06
07
08
09
10
11
UP HOSE ORDERING ENGINE (UPE)
TLB BLOCK (TLB)
DOWN HOSE FORWARD INITIATOR (DFI)
MASK 8b x 192w
ERROR
UP HOSE DATA (WBF) 64b x 224w
IO7 INTERNAL CSR DATA (CSR)
HOT PLUG (HPLG)
DOWN HOSE DATA (RBF) 66b x 224w
DOWN HOSE ADD (DNA) 82b x 8w
DOWN HOSE ORDERING ENGINE (DNE)
UNORD.
ORD.
RAP BDR
FWD ADDRESS
UP DATA
DOWN DATA
DOWN ADDRESS
TO (UPE)
agp/pci_ addr_in
csr_data FROM csr.tlb.bplg
DOWN DATA
pci_addr_out
DOWN HOSE PACKET DONE
addr_in
pci_data_in
PCI/PCI-X (PCX)
addr_in
AGP_sha_in
AGP_ad_in
AGP_ad_out
PCI_ad_in
PCI_ad_out

FIG. 8

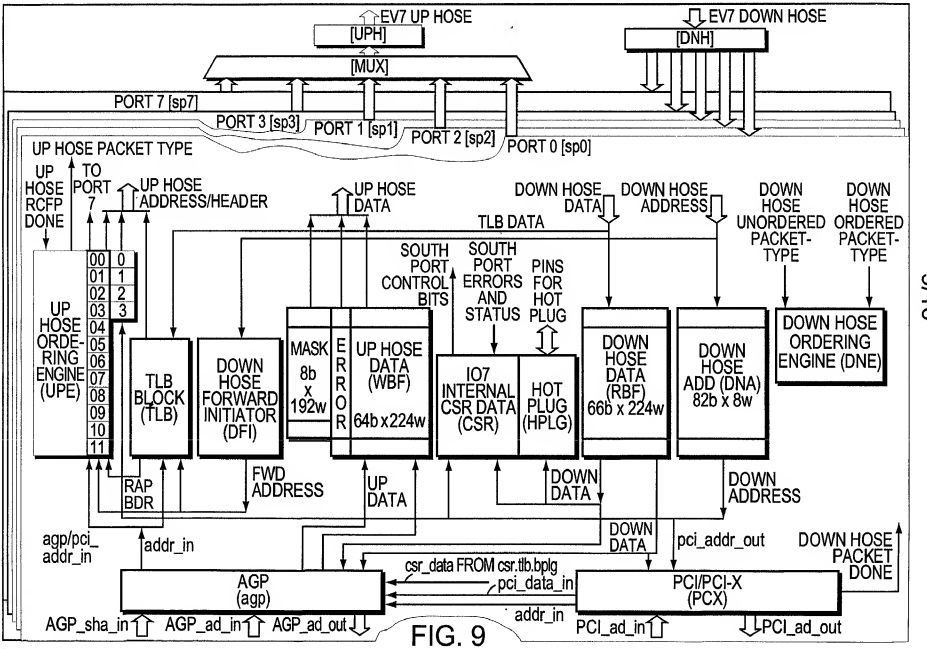
EV7 UP HOSE
[UPH]
EV7 DOWN HOSE
[DNH]
[MUX]
PORT 7 [sp7]
PORT 3 [sp3]
PORT 1 [sp1]
PORT 2 [sp2]
PORT 0 [sp0]
UP HOSE PACKET TYPE
UP HOSE RCFP DONE
TO PORT 7
UP HOSE ADDRESS/HEADER
UP HOSE DATA
DOWN HOSE DATA
DOWN HOSE ADDRESS
DOWN HOSE UNORDERED PACKET-TYPE
DOWN HOSE ORDERED PACKET-TYPE
TLB DATA
SOUTH PORT CONTROL BITS
SOUTH PORT ERRORS AND STATUS
PINS FOR HOT PLUG
00 0
01 1
02 2
03 3
04
05
06
07
08
09
10
11
UP HOSE ORDERING ENGINE (UPE)
TLB BLOCK (TLB)
DOWN HOSE FORWARD INITIATOR (DFI)
MASK 8b x 192w
ERROR
UP HOSE DATA (WBF) 64b x 224w
IO7 INTERNAL CSR DATA (CSR)
HOT PLUG (HPLG)
DOWN HOSE DATA (RBF) 66b x 224w
DOWN HOSE ADD (DNA) 82b x 8w
DOWN HOSE ORDERING ENGINE (DNE)
RAP BDR
FWD ADDRESS
UP DATA
DOWN DATA
DOWN ADDRESS
agp/pci_ addr_in
addr_in
DOWN DATA
pci_addr_out
DOWN HOSE PACKET DONE
csr_data FROM csr.tlb.bplg
pci_data_in
AGP (agp)
PCI/PCI-X (PCX)
addr_in
AGP_sba_in
AGP_ad_in
AGP_ad_out
PCI_ad_in
PCI_ad_out

FIG. 9

1500

POx_CTRL

NAME	EXTENT	ACCESS	INITIAL STATE	FIRMWARE INITIAL STATE	
CACHE_ LINE_LEN	7:0	RW	40	MUST BE 40	CACHE LINE SIZE. USED BY MEGACELL FOR PCI-2.2 LATENCY TIMER EXPIRATION DURING MWI CYCLES. csr2xcal_cacheline_size (7:0)
DIS_ 64BIT_BUS	8	RW	0	0	0: BUS IS 64 BITS WIDE 1: BUS IS 32 BITS WIDE THIS BIT CONTROLS DRIVING REQ64 AT RELEASE OF RESET. MEGACELL ASSUMES THIS IS THE VALUE OF REQ64 LATCHED ON RISING EDGE OF pci_reset. USED TO DETERMINE PCI(X) 64-BIT BUS CAPABILITY. (csr2xcal_64bit_bus_en_n). THIS BIT MUST BE SET (BY FIRMWARE) ON PORT 3.
DIS_ ACK64	9	RW	0	0	0: ENABLE 64-BIT TARGET CAPABILITY ON THIS PORT 1: DISABLE 64-BIT TARGET CAPABILITY (csr2xcal_64bit_tgt_en_n). THIS BIT MUST BE SET (BY FIRMWARE) ON PORT 3.
DIS_ REQ64	10	RW	0	0	0: ENABLE 64-BIT INITIATOR CAPABILITY 1: DISABLE 64-BIT INITIATOR CAPABILITY (csr2xcal_64bit_initr_en_n). THIS BIT MUST BE SET (BY FIRMWARE) ON PORT 3.
DIS_ BURST	11	RW	0	0	0: ENABLE PCI INITIATOR BURST CAPABILITY. 1: DISABLE PCI INITIATOR BURST CAPABILITY. (csr2xcal_64bit_initr_en_n)
RESERVED	14:12	RAZ	0	0	
EN_ IO7_PARK	15	RW	0	0	0: PARK GNT ON LAST MASTER 1: PARK GNT ON IO7
Spl_ Cmp_MSG	19:16	RW	0		SPLIT COMPLETION MESSAGE. THIS FIELD IS WHAT IO7 WILL PROVIDE IN THE DEVICE SPECIFIC FIELD OF A SPLIT COMPLETION MESSAGE.
EN_ MSTR_LT	20	RW	0	1	0: FOLLOW THE PCI SPEC FOR MASTER LATENCY (EXCEPTION: DISCONNECT AT CACHE LINE BOUNDARIES) 1: IGNORE THE MASTER LATENCY TIMER csr2xcal_lattmr_disable

FIG. 10A

NAME	EXTENT	ACCESS	INITIAL STATE	FIRMWARE INITIAL STATE	
EN_ PCHK	21	RW	0	1	DISABLES CHECKING PARITY ON AD(63::00) AND C/BE(7::0)# DURING PCI ADDRESS AND DATA PHASES. csr2xcal_par_en
RESERVED	22	RAZ	0	0	
EN_TLB_ CACHE	23	RW	0	1	IF SET TLB ENTRIES WILL BE CACHE COHERENTLY. IF CLEAR TLB ENTRIES WILL BE FETCHED AND TRANSLATIONS DISCARDED AFTER FIRST USE. csr2tlb_eache_ena
RESERVED	25:24	RAZ	0		
EN_ASSERT_ SERR	26	RW	0	0	ENABLE SERR ASSERTION ON PCI(X) BUS. csr2p_serr_en THIS BIT HAS UNEXPECTED SIDE EFFECTS IN THE X-CALIBER CORE. IO7 WILL CORRECTLY DETECT AND LOG COMMAND/ ADDRESS/ATTRIBUTE PARITY ERRORS WITH THIS BIT CLEAR AND WILL TARGET ABORT THE EFFECTED TRANSACTION. UNWANTED SIDE EFFECTS OF SETTING THIS BIT INCLUDE ASSERTION OF SERR# WHEN THE TARGET OF A PIO WRITE ASSERTS PERR#.
RESERVED	27	RAZ	ZOS		
RM_TYPE	29:28	RW	01	01	CONTROL THE PREFETCH ALGORITHM USED FOR PCI MEMORY READ MULTIPLE COMMAND. 00 = TWO DMA STATE MACHINES (ALLOWS EVEN DISTRIBUTION FOR A HEAVILY POPULATED BUS) 01 = SIX DMA STATE MACHINES (DEFAULT) 10 = EIGHT DMA STATE MACHINES (FOR BETTER SINGLE STREAM PERFORMANCE) 11 = ELEVEN DMA STATE MACHINES (NEVER ALLOW 12 ON A READ)

1502

FIG. 10B

NAME	EXTENT	ACCESS	INITIAL STATE	FIRMWARE INITIAL STATE	
DIS_FUNK_ ALIAS	30	RW	0	0	0: ALLOW IO7 TO IDENTIFY ITSELF USING MULTIPLE FUNCTION NUMBERS IN PCI-X 1: IO7 USES ONLY ONE FUNCTION NUMBER
EN_AGP_ RD_CACHE	31	RW	0	0	THIS MUST ALWAYS BE SET TO 0 ON PORT 3 0: DISABLE PREFETCH DATA CACHE (ONLY USE FETCH COMMANDS) FOR PCI DMA READ DATA 1: ENABLE PREFETCH DATA CACHE (USE PREFETCH COMMANDS)
EN_ PREFETCH	32	RW	0	1	0: NO PREFETCH; FETCH MINIMUM ONLY 1: USE PREFETCH PREDICTION
RESERVED	34:33	RAZ	ZOS	0	
PCI_ARB_ MODE	36:35	RW	0	0	0: ROUND ROBIN 1: IO7 PRIORITY MODE: IO7 IS GIVEN THE HIGHEST PRIORITY AND IS GRANTED THE BUS WHENEVER IT IS REQUESTED. WHEN IO7 IS NOT REQUESTING THE BUS IT IS ROUND ROBIN. 2: BUS HOG MODE: DEVICE 0 (`SLOT 0') IS GIVEN HIGHEST PRIORITY AND IS GRANTED THE BUS WHENEVER IT IS REQUESTED. OTHERWISE IT IS ROUND ROBIN. PEER TO PEER IS NOT SUPPORTED TO OR FROM THE `BUS HOG' DEVICE. UPE_PCI_22_ MODE MUST BE 0 (STRICT ROUND ROBIN) WHEN RUNNING IN BUS HOG MODE. 0: RESERVED
EN_PCI_ RD_CACHE	37	RW	0	0	THIS SHOULD BE SET TO 0 ON PCI-X AND TO 1 OR 0 ON PCI BUSES, csr2upe_en_rd_cache 0: DISABLE PREFETCH DATA CACHE (ONLY USE FETCH COMMANDS) FOR PCI DMA READ DATA 1: ENABLE PREFETCH DATA CACHE (USE PREFETCH COMMANDS)

FIG. 10C

NAME	EXTENT	ACCESS	INITIAL STATE	FIRMWARE INITIAL STATE		
UPE_PCI_22_MODE	38	RW	0	0	PCI 2.2 READ RETURN (DOWN HOSE) ORDERING COMPLIANT MODE: csr2upe_pel_22_mode 0 = STRICT ROUND-ROBIN (DMA/PPR FILLS MAY PASS PIO/PPR WRITES) 1 = IO7 PRIORITY MODE (2.2 COMPLIANT) (DMA/PPR FILLS SHALL NOT PASS PIO/PPR WRITES)	
UPE_ENG_EN<11:0>	50:39	RW	0	FFF	ENABLE UP STATE MACHINE ENGINES; ONE BIT PER ENGINE. NOTE: WHEN THERE IS PEER-TO-PEER READ TRAFFIC AT LEAST TWO ENGINES MUST BE ENABLE. THIS RESERVATION IS TO AVOID DEADLOCK - WRITES ALWAYS MAKE PROGRESS. ALSO NOTE: PORT 3 MUST HAVE AT LEAST 4 ENGINES ENABLE, UPE_ENG_EN<3:0> TO SUPPORT "AGP LONG READS" AND TO LIMIT PCI TO ENGINES <11:4>. USE THIS FIELD TO CAUSE IO7 DMA TO GO QUIESCENT IN SUPPORT OF HOT ADD OR SWAP OF A CPU. csr2upe_eng_en(11:0)	1504
ENA_AGP_ORDER	51	RW	1	1	THIS BIT EFFECTS PORT 3 ONLY 1: USE AGP ORDERING RULES (UP HOSE READS MAY BYPASS WRITES) 0: USE PCI ORDERING RULES	
UPE_PPRWR_RX	52	RW	0	0	RELAX ORDERING FOR PPR WRITES: 0 - PEER WRITES ARE NOT ORDERED WITH RESPECT TO OTHER PEER WRITES 1 - PEER WRITES ARE ORDERED BY LIMITING TO ONE AT A TIME. csr2upe_pprwr_rx	1501
HPCE_ENA	53	RW	0		SET TO ENABLE EXTERNAL HOT PLUG LOGIC.	
RESERVED	60:54	RAZ	0	0		

FIG. 10D

NAME	EXTENT	ACCESS	INITIAL STATE	FIRMWARE INITIAL STATE	
AGP_MW	61	RW	0	1	0: SBA48 IS LOGICAL "OR" OF SBA ADDRESS BITS 47:32 (USE WINDOW 3 AS 4G SCATTER/ GATHER TARGET) 1: SBA49 ALWAYS SET (AGP USES MONSTER WINDOW ONLY) csr2agp_mw ONLY MEANINGFUL ON PORT 3
AGP_RD_ CONCAT	62	RW	0	1	ENABLE CONCATENATION OF READS FROM AGP csr2agp_rd_concat ONLY MEANINGFUL ON PORT 3
AGP_WR_ CONCAT	63	RW	0	1	ENABLE CONCATENATION OF WRITES FROM AGP csr2agp_wr_concat ONLY MEANINGFUL ON PORT 3

FIG. 10E

1600

NAME	EXTENT	ACCESS	INITIAL STATE	FIRMWARE INITIAL STATE		
UPH_PID	10:0	RW	x400		PID<9:0> = PID OF THIS DEVICE USED IN ALL REQUEST PACKETS. NOTE THAT PID<9> IS ALWAYS SET TO 1 FOR IO7. csr2uph_pid (10:0)	
UPH_CD_REQ	15:11	RW	0		UP HOSE BUFFER CREDITS: Req csr2mux_crdt_req(4:0)	1602a
UPH_CD_RIO	20:16	RW	0		RdIO csr2mux_crdt_rio(4:0)	1602b
UPH_CD_WIO	25:21	RW	0		WrIO csr2mux_crdt_wio(4:0)	1602c
UPH_CD_BLK	30:26	RW	1		BlkResp csr2mux_crdt_blk(4:0)	1602d
UPH_CD_NBK	35:31	RW	1		NoBlk csr2mux_crdt_nbk(4:0)	1602e
UPH_FR_CNT	36	RW	0		csr2uph_fr_cnt 0: FORCE ERRORS AS ONE-SHOT, SINGLE FLIT ASAP. IN THIS MODE THE UPH_FR_xxx BIT IS CLEARED BY HARDWARE AFTER THE ERROR IS POSTED. 1: FORCE ERRORS ONCE EVERY 2nd FORWARD CLOCK TICKS	
UPH_FR_HDR	37	RW	0		csr2uph_fr_hdr 0: FORCE ERRORS ON DATA FLIT 1: FORCE ERRORS ON HEADER FLIT	
UPH_FR_SBE	38	RW	0		FORCE: SINGLE BIT ERROR csr2uph_fr_sbe	
UPH_FR_DBE	39	RW	0		DOUBLE BIT ERROR csr2uph_fr_dbe	
UPH_FR_GBG	40	RW	0		GARBAGE CODE csr2uph_fr_gbg	
UPH_ARB_MODE	42:41	RW	0		CONTROLS PRIORITY OF AGP RELATIVE TO OTHER PORTS. (PORT 7 IS FIRST BECAUSE ALL FWD-MISSES COME THROUGH IT). 0 - PORT 7 FIRST; ROUND ROBIN 0,1,2,3 1 - PORT 7 FIRST, PORT 3 SECOND, ROUND ROBIN 0,1,2 2:3 - RESERVED	
RESERVED	63:43	RAZ	0			

1602

FIG. 11

1700

NAME	EXTENT	ACCESS	INITIAL STATE	FIRMWARE INITIAL STATE	
UPE_FLUSH_CACHE	0	W/RAZ	0	0	SET TO INVALIDATE ALL (FETCHED) NON-COHERENT BLOCKS. VictimClean COHERENT BLOCKS. SET BY WRITE OR AS A SIDE EFFECT OF FAULT RESET. THIS APPEARS THE SAME AS A FORWARD HIT ON ALL CACHED DATA. csr2upe_flush_cache
UPE_CACHE_INV	1	RO	0		SET WHEN ONE OR MORE BLOCKS IN TLB, READ AND WRITE CACHES ARE VALID (A PENDING REQUEST, VICTIM OR DIRTY DATA) NOTE - THIS MAY NEVER CLEAR IF THERE IS AN ERROR. IN ERROR CASE JUST PCI_RESET.
RESERVED	2	RAZ	0		
PCI_RESET	3	RW	0	1	1: PCI RESET NOT ASSERTED 0: PCI RESET ASSERTED
RESERVED	63:41	RAZ	0		

1702

1704

FIG. 12